

Thunderbolt™ Release Notes For Burnside Bridge A-Step for Tiger Lake SoC

Release Notes - NDA

January 2020

Revision 7.0

Intel Confidential



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Audience

This document intended for use by OEM software developers, test and validation engineers, and system integrators.



Contents

1	Introduction	6
	1.1 Scope of Document	6
	1.2 Acronyms	6
	1.3 Naming Convention:	7
	1.4 Lane N/P Swap configuration	7
2	Release Summary	8
	2.1 Release Overview	8
3	Features Supported	9
	3.1 Best Known Configuration	9
4	New Features–RCRs	10
5	Issue Status Definitions	11
	5.1 Fixed Issues in This Release	12
	5.2 Known Issues–To Date	13
	5.3 Archive–Fixes in Previous Releases	14



Revision History

Revision Number	Description	Revision Date
1.0	Engineering release for Burnside Bridge Rev 1.0 for Tiger Lake	June ,2019
2.0	Engineering release for Burnside Bridge Rev 2.0 for Tiger Lake	August ,2019
4.0	Engineering release for Burnside Bridge Rev 4.0 for Tiger Lake	September ,2019
5.0	Engineering release for Burnside Bridge Rev 5.0 for Tiger Lake	November ,2019
7.0	Engineering release for Burnside Bridge Rev 7.0 for Tiger Lake	January ,2020



1 Introduction

1.1 Scope of Document

This document provides component-level details of the downloaded release and the contents of each folder in the release.

1.2 Acronyms

Term	Description
TBT	Thunderbolt™
HR	Host Router
EP	End Point
AIC	Add-In Card
PR	Port Ridge (Thunderbolt™)
FR	Falcon Ridge (Thunderbolt™ 2)
AR	Alpine Ridge (Thunderbolt™ 3)
TR	Titan Ridge (Thunderbolt™ 3)
DP	Display Port
CM	Connection Manager
LC	Link Controller
HDCP	High-bandwidth Digital Content Protection
DB	Delta Bridge – TBT Retimer
BB	Burnside Bridge – TBT Retimer
ICL	Intel Ice Lake SoC
TGL	Intel Tiger Lake SoC



1.3 Naming Convention:

<project name>_<mode>_<Si stepping>_<image rev>.bin

For example

<project name>:

LR, PR, AR, TR, etc.

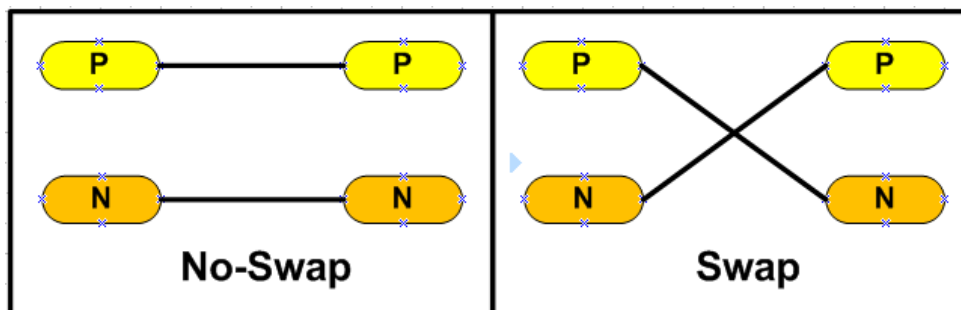
<mode>:

OB = Onboard

BB_CDR_A0_Rev10.bin – Burnside Bridge A0 stepping Revision 10

1.4 Lane N/P Swap configuration

Note: Each revision might have different instructions on how to control board-dependent channels lanes N/P swap configuration.





2 Release Summary

This document covers Thunderbolt™ Firmware for the Burnside Bridge A-Step Retimer for Tiger Lake based platforms only.

2.1 Release Overview

The release can be downloaded from **Intel VIP** (<https://platformsw.intel.com/>).

Note: Please use **Thunderbolt Retimer Tool** latest version (**Doc ID#: 597797**) from **My Intel** to configure retimer firmware correctly.

Note: A username and password are required to access the website and to log in. The user must have an account created for access.



3 Features Supported

Supported = ✓ Limited Support = ⚠ Not Supported = ✗

Technology	Support
Thunderbolt™ Link 20/40G	✓
Thunderbolt™ Link Power Management (CLx)	✓
SMBUS	✓
LTTPR	✓
DSC/FEC	✓
DisplayPort	✓
vPro over Thunderbolt™	✓
USB™ 3 10G/5G	✓
USB™ 4	✓
Sx	✓
Wake	✓
Firmware update – TBT system	✓
RTD3	✓

3.1 Best Known Configuration

For the latest client-based platforms Best Known Configuration (BKC), please contact your platform CE



4 *New Features–RCRs*

RCR #	Title	Change Info	Status



5 *Issue Status Definitions*

This document provides sightings and bugs report for Thunderbolt™ Burnside Bridge SKUs. At the time of a milestone release, this report will be distributed with the Intel® TBT Release and will provide information on new issues and the status of old issues (replacing the Release Notes document).

Closed Issues: This category will only display closed issues within the current Intel® TBT release. After each release, old issues will be dropped down to the “Archive” section and then new closed issues will take its place back up top for the next release. If an issue is posted in this section, it will indicate that the issue has been verified and fixed within the one that is being released.

Known Issues: This category will display all Known Issues since the initial release and will remain in this section until fixed or noted otherwise. “Known Issues” are still under investigation and may or may not be root caused.

Archive – Fixes in Previous releases: This category will display all closed issues that were closed in their respected release#. This section will serve as a history of fixed issues.

Sightings listed in this document apply to the Thunderbolt™ Burnside Bridge SKUs unless noted otherwise in this document or in the sightings tracking systems.



5.1 Fixed Issues in This Release

Issue Closed in Release #	Title	Details
7.0	USB-C ethernet adapter uses a self-assigned IP after wake from S0ix.	Sighting #: 5324450 Affected Component: LC Impact: Delay around the Sx exit. Fix: Abort I2C slave delay when USB is connected.
7.0	DP AUX Channel	Sighting #: 5324453 Affected Component: LC Impact: AUX is coming from different sources and not via SBU lines. Fix: Disconnect AUX on port close to SoC.



5.2 Known Issues–To Date

Issue Found in Release #	Title	Details



5.3 Archive–Fixes in Previous Releases

Issue Fixed in Release #	Title	Details
5.0	USBC fail TD 4.1.1 Initial Voltage Test on LeCroy	Sighting #: 2208232640 Affected Component: LC Impact: USBC fail TD 4.1.1 Initial Voltage Test on LeCroy. Fix: The test specification will change to ensure CC terms are presented and DUT is in DFP role to ensure retimers that are PG are brought out of reset. Disconnect 1M PD on all ports except the connector port, in disconnect.
5.0	RTD3 wake from LAN fail	Sighting #: 1306641541 Affected Component: LC Impact: RTD3 wake from LAN fail. Fix: Reset RTD3 entry state on vPro time out during Sx.
5.0	FEC Enable Alignment	Sighting #: 1507279159 Affected Component: DP Impact: Some DP sinks (monitor, MST, etc.) won't work because of bad FEC indication. Fix: Reply the FEC enable reflecting indication from both the Ridge and the target sink.
5.0	Debounce Indication	Sighting #: 1409525414 Affected Component: DP Impact: The Monitor Display Mode cannot keep <i>PC Only Mode</i> when Type-C to HDMI dongle is used. Through some MFDP dongles " <i>Show only on external screen</i> " does not work. Fix: Debounce indication to LC, if <i>Sink_Count</i> is 0.
5.0	DPCD Write Fix	Sighting #: N/A Affected Component: DP Impact: When connected to old GPUs some monitors won't work due to unusual flow. Fix: Add FW robustness to handle unusual <i>DPCD 0x102</i> writes on certain GPUs.
2.0	TBT File transfer during RTD3 exit	Sighting #: 5324439 Affected Component: LC Impact: In RTD3 exit there is a timeout by CM for sending the topology connected to the BIOS, therefore the file transfer fails after RTD3 exit. Fix: Remove LC delay for 50ms in this case to be able to bring up the link on time.
1.0	TBT connection while system is in Sx	Sighting #: 5324427 , 2207488704 Affected Component: LC Impact: Retimer does not wake up when the system exits Sx/G3 causing enumeration failure on G3. Fix: The retimer FW changed to monitor GPIO 6 only that serves as indication that system enters S0 state.