

TIGERLAKE TSN
ADD IN CARD (PHASE 2)
FAB A

TA : K81998-100
AA : K82000-100
PBA: K81999-100
PB : K82001-100

DEAR CUSTOMER LETTER: K82003-001
USER MANUAL : K82002-001
SAFETY WARNING FLYER: K82004-001

LB1L1 BOARD SERIAL NUMBER
LABEL

SERIAL NUMBER

J62945-001

LB1M1
EMPTY

WEEE

LB1M2
EMPTY



LABEL_CHINA_ROHS_10

| INTEL CONFIDENTIAL INFORMATION | | | |
|--|--------------------------|---------|---------------|
| <div>INTEL CORPORATION</div> <div>2111 NE 25th Ave.</div> <div>Hillsboro, Oregon</div> <div>TOOLS OPTIONS CUSTOM VARIABLES</div> | | | |
| PROJECT TITLE: | TGL TSN AIC (PH2) | | |
| SHEET SIZE: | A3 | PBA NO: | K81999-100 |
| REVISION: | 0p98 | | |
| DATE: | Wed Dec 18 14:47:09 2019 | | PAGE: 1 OF 23 |

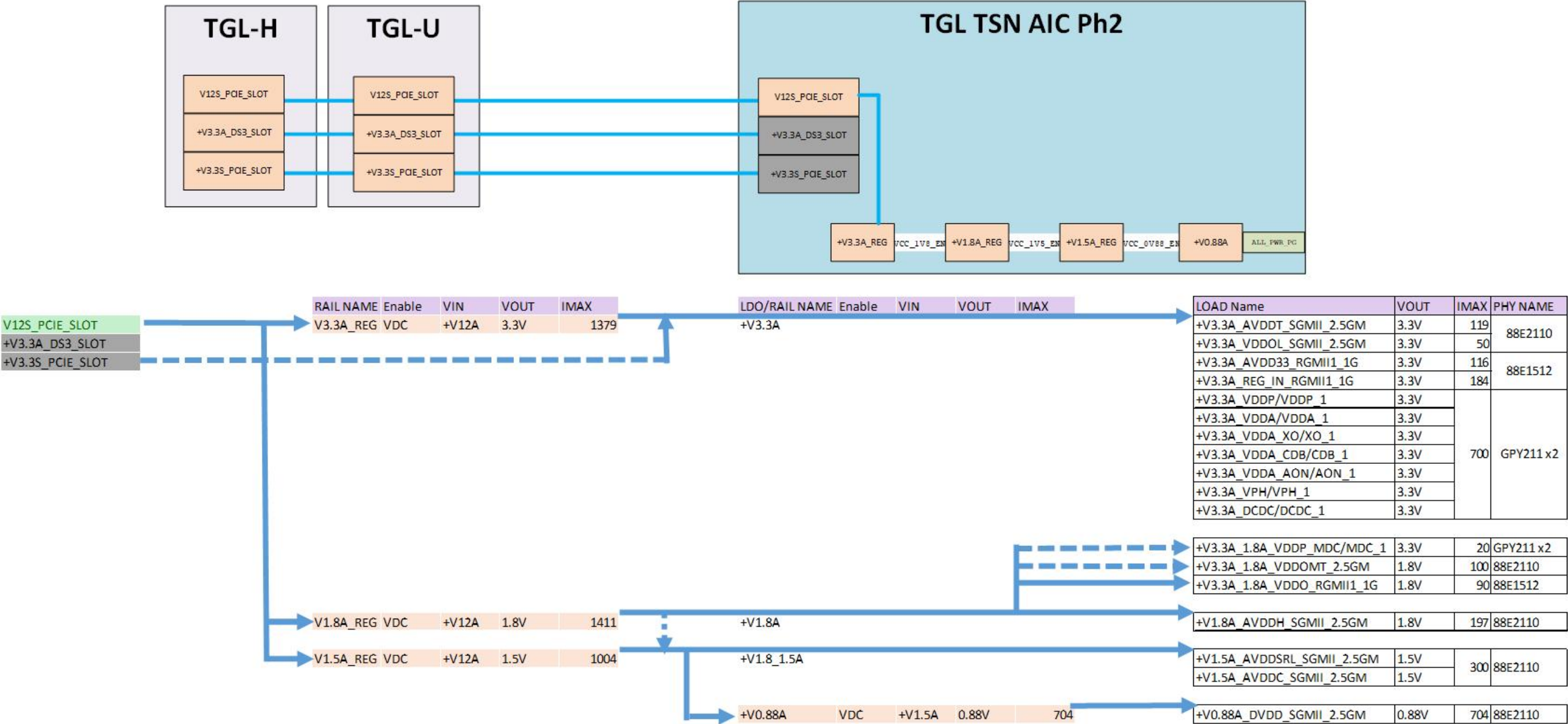
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|--|---------------------------|------------|--|--------------------------------|--|------|--|--------------------|--|---------------|--|
| CR-2 : @TGLTSNAICPH2_LIB.TGLTSNAICPH2(SCH_1):PAGE2 | | | | 4 | | 3 | | 2 | | 1 | |
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| INTEL CONFIDENTIAL | | | | | | | | | | | |
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CONFIG OPTION

DEFAULT

| TSN PH2 AIC Configuration | For | Board PCIE Slot | | Board PCIE Lane Pin Name | | MDC/MDIO thru | AIC PHY stuffing (Bold Default) |
|---------------------------|-------|-----------------|----|------------------------------|------------------------------|----------------------------|---|
| PET/R 0:1 | TGL H | J8B1 | X4 | PCIE_9_LAN_0B_TSN_0_TX/RX | PCIE_10_TSN_1_TX/RX | TBD | 88E1512 /GPY211 + 88E2110 /GPY211 |
| | TGL U | J8B1 | X1 | PCIE3_P8_LAN_0B_TSN_0B_TX/RX | NC | PCIE SMBus + NC | 88E1512 /GPY211 + NC |
| PET/R 2:3 | TGL U | J7B1 | X4 | PCIE3_P7_LAN_0A_TSN_0A_TX/RX | PCIE3_P8_LAN_0B_TSN_0B_TX/RX | Header + PCIE SMBus | 88E1512 /GPY211 + 88E2110 /GPY211 |

POWER MAP



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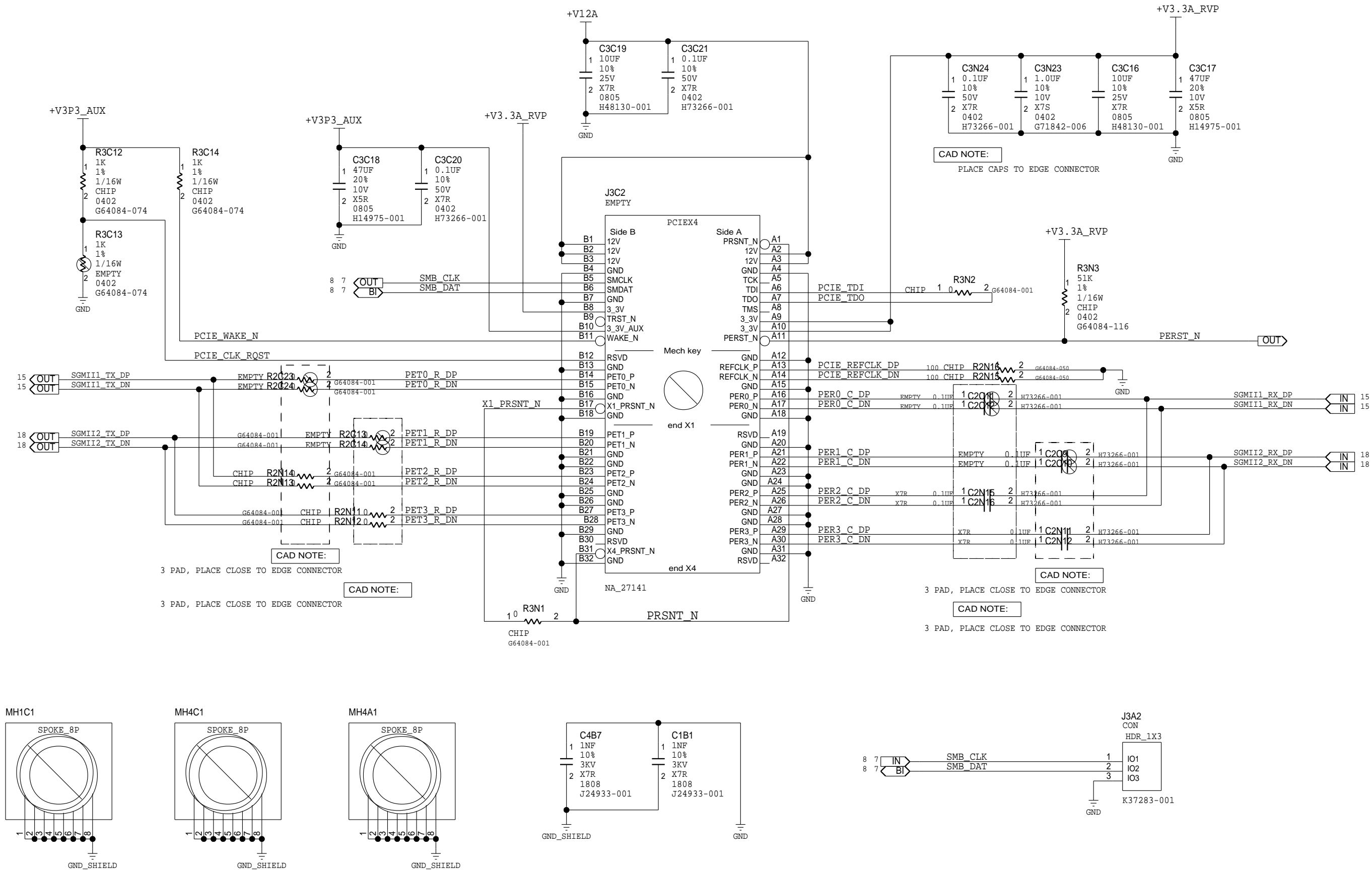
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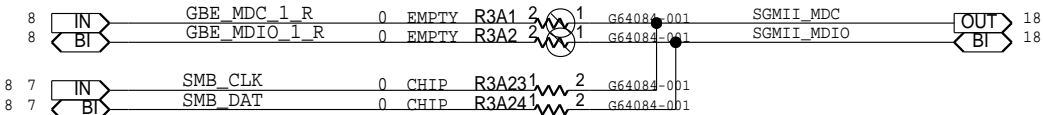
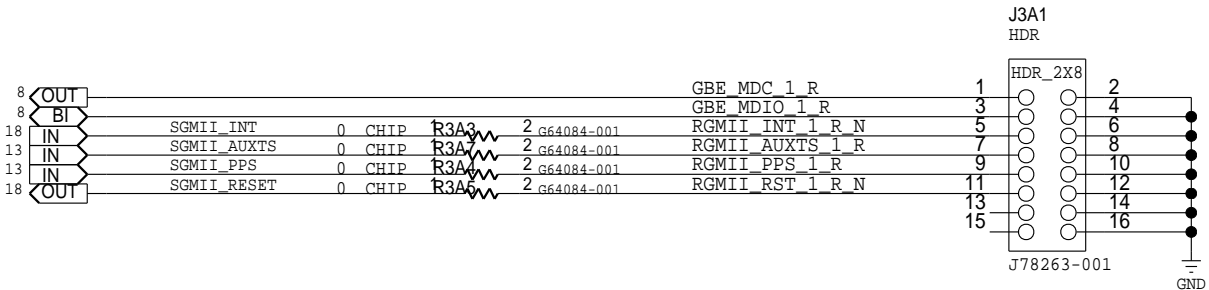
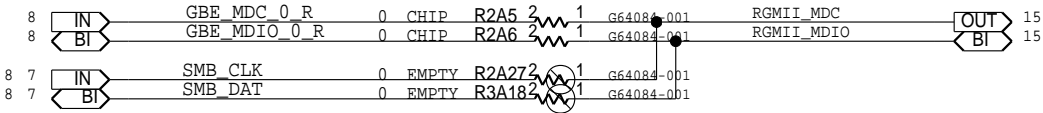
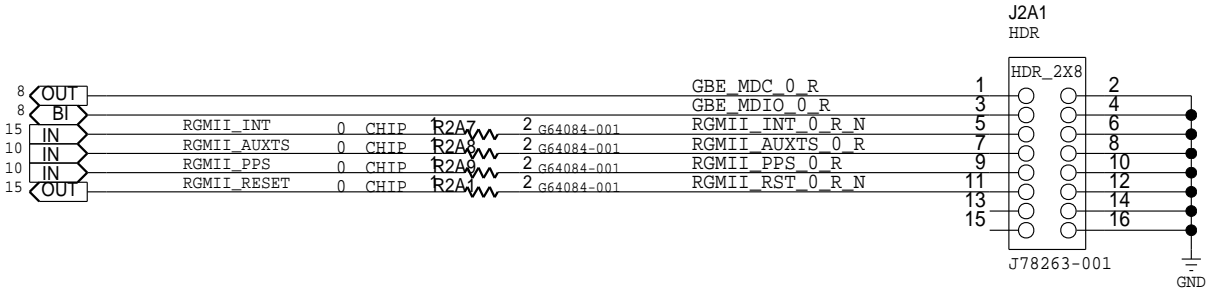
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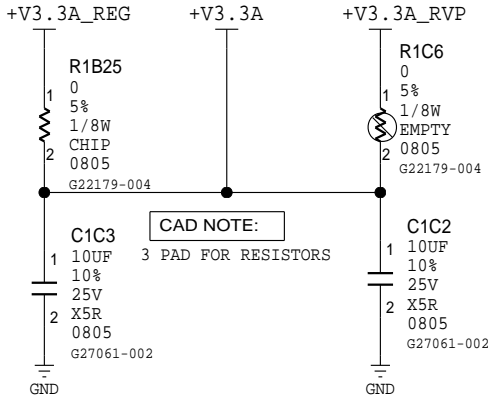
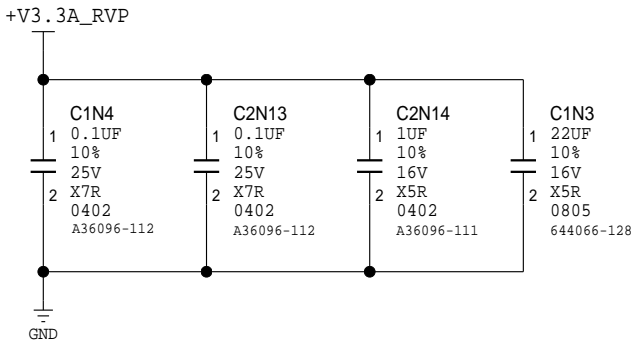
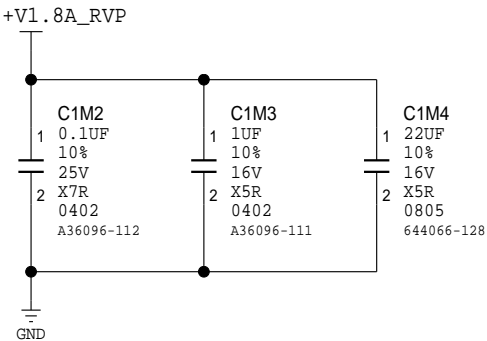
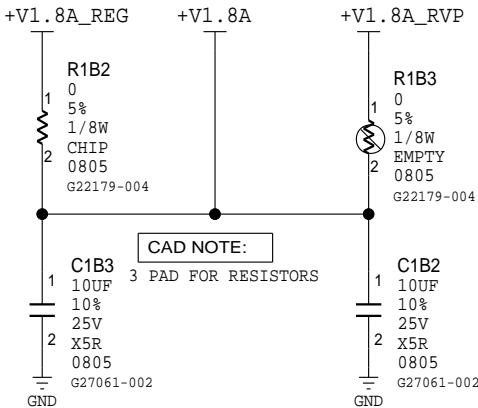
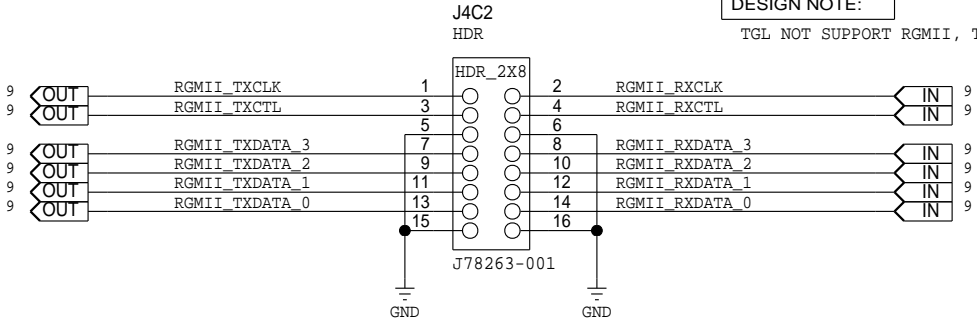


ALL RGMII* SIGNALS ARE ON 1.8V DOMAIN
RGMII_AUXTS: AUXILLARY TIME STAMP TRIGGER. EDGE SENSITIVE. TRIGGERS STORING TIME STAMP IN A 4X64 DEEP FIFO ON RISING EDGE
RGMII_INT: EXTERNAL INTERRUPT FROM RGMII PHY OR SGMII PHY. ALSO USED FOR WOL. THIS IS ALSO ROUTED TO PMC FOR WOL IN SOIX
RGMII_RESET: RGMII OR SGMII PHY RESET
RMII_PPS: PULSE PER SECOND FOR RGMII OR SGMII PHY SYNC



DESIGN NOTE:

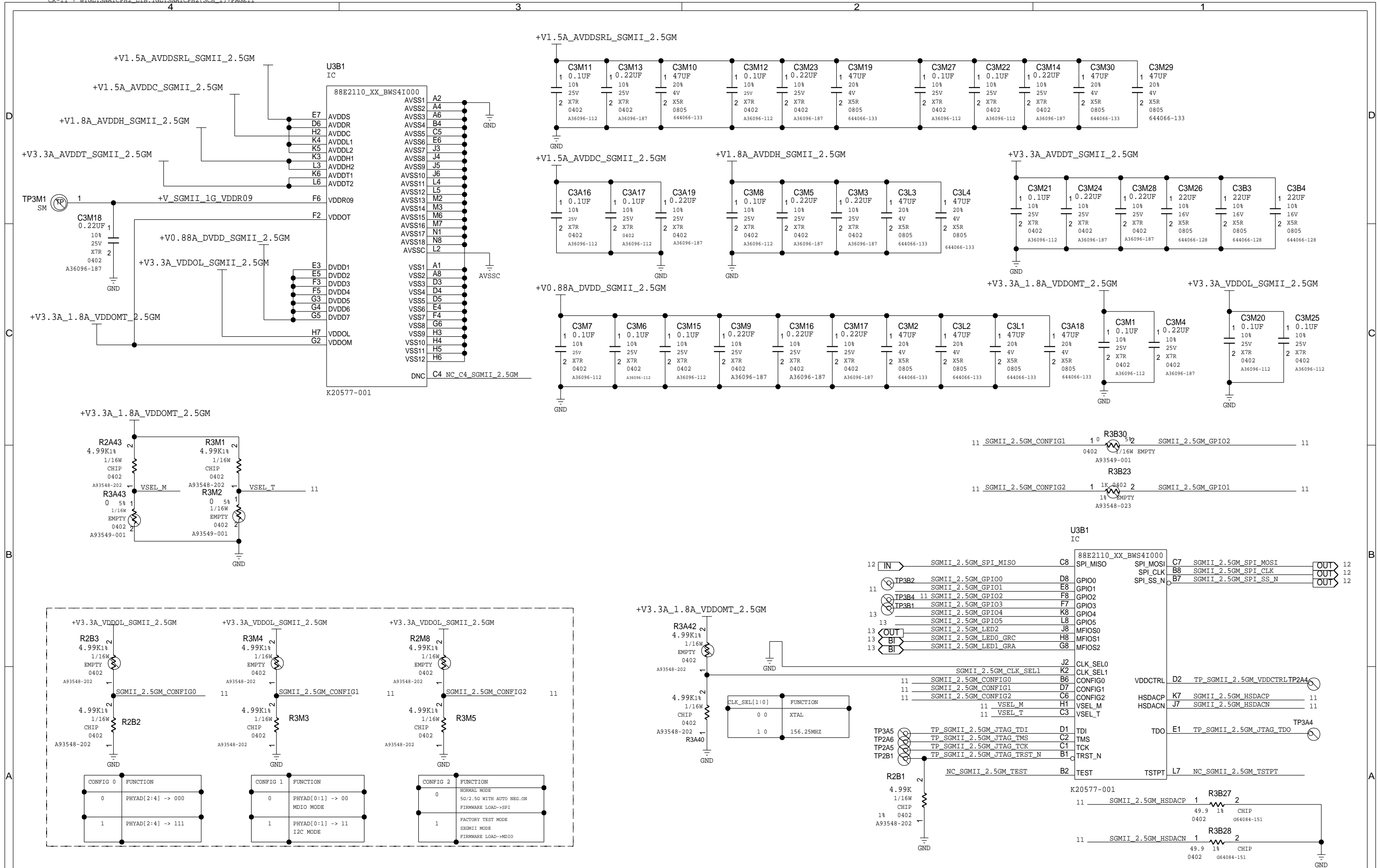
TGL NOT SUPPORT RGMII, THIS HEADER IS FUTURE PROOF FOR OTHER PLATFORM

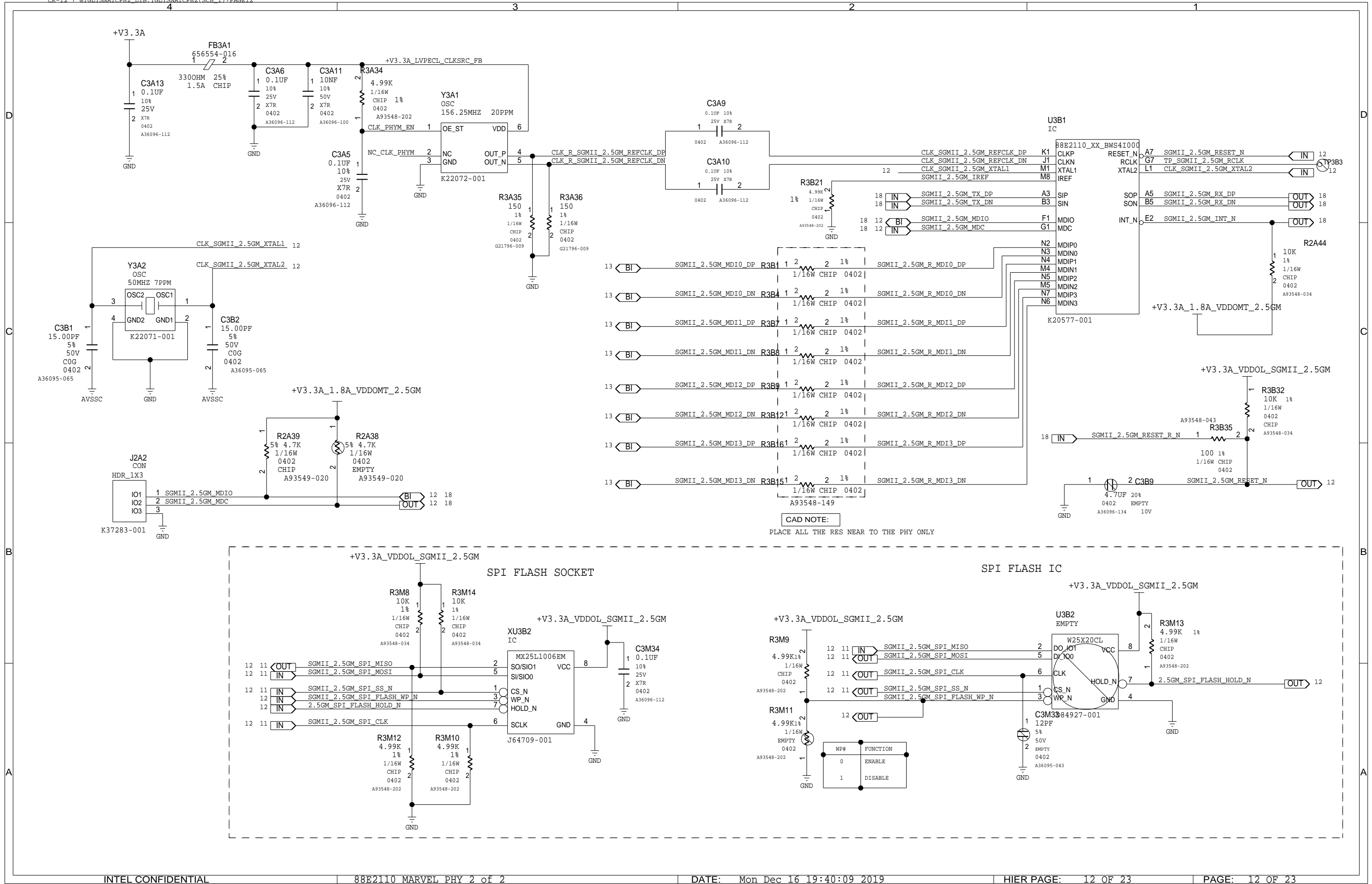




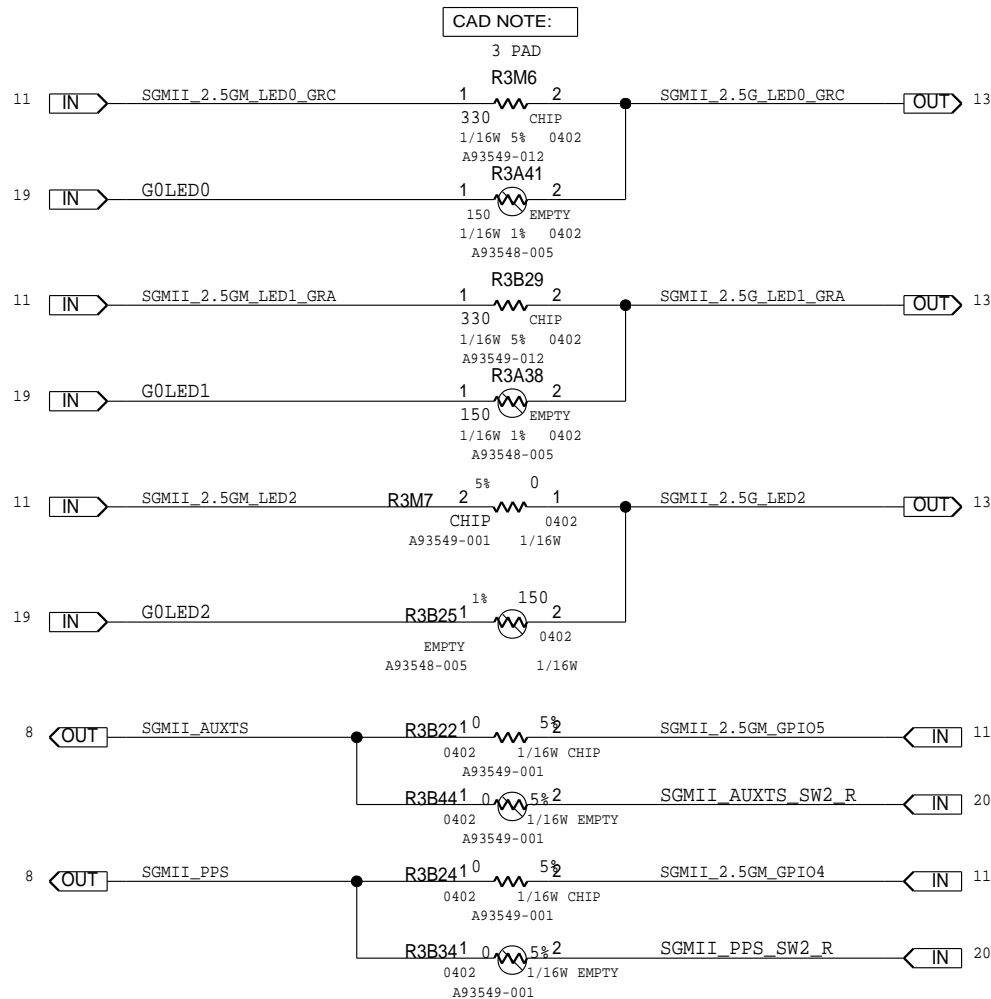
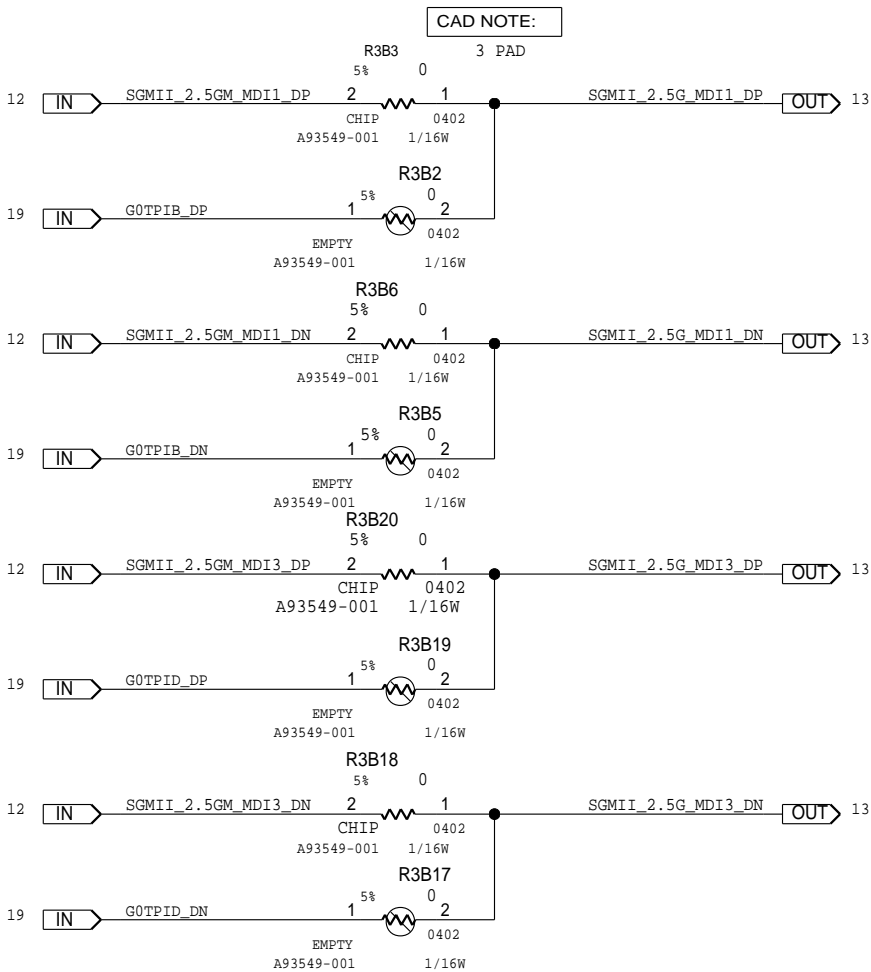
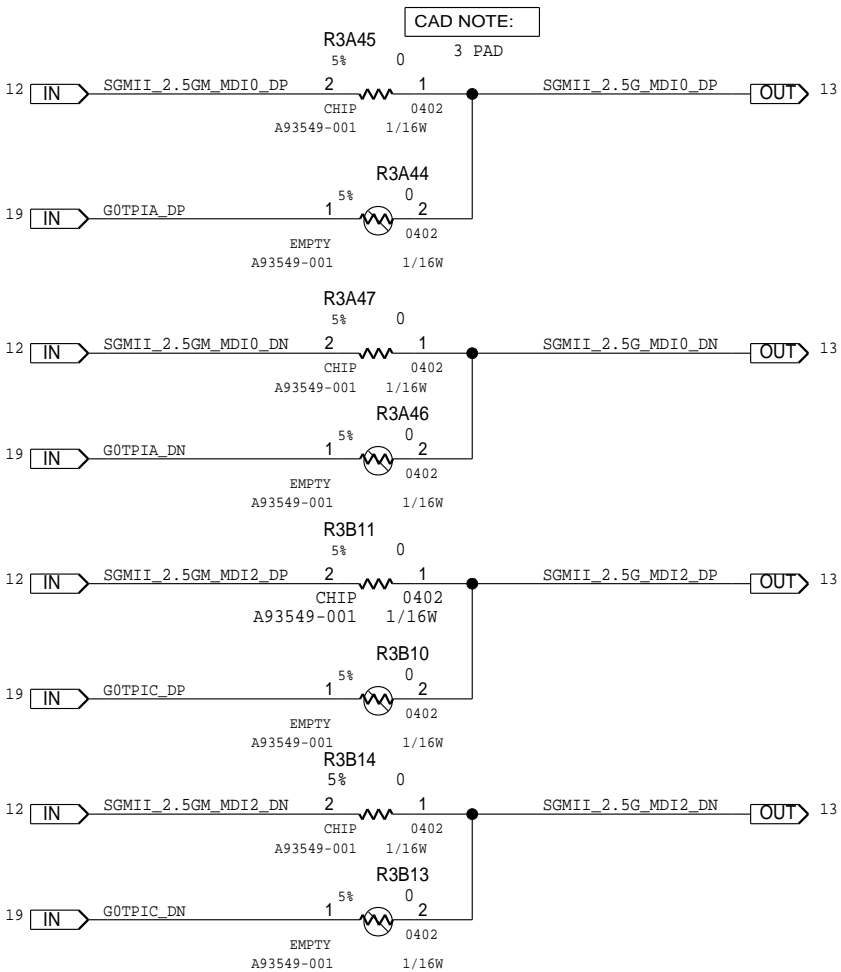
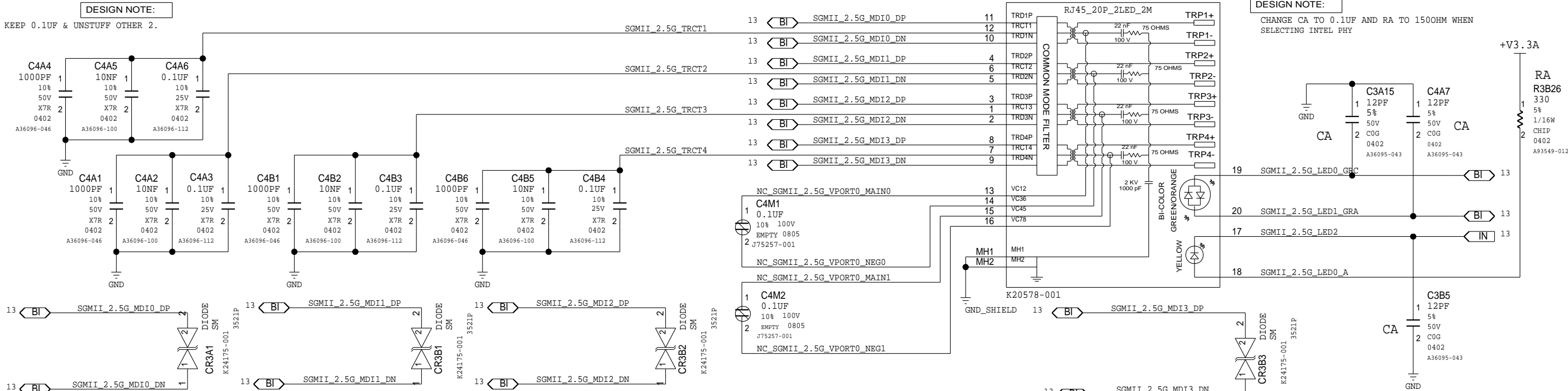
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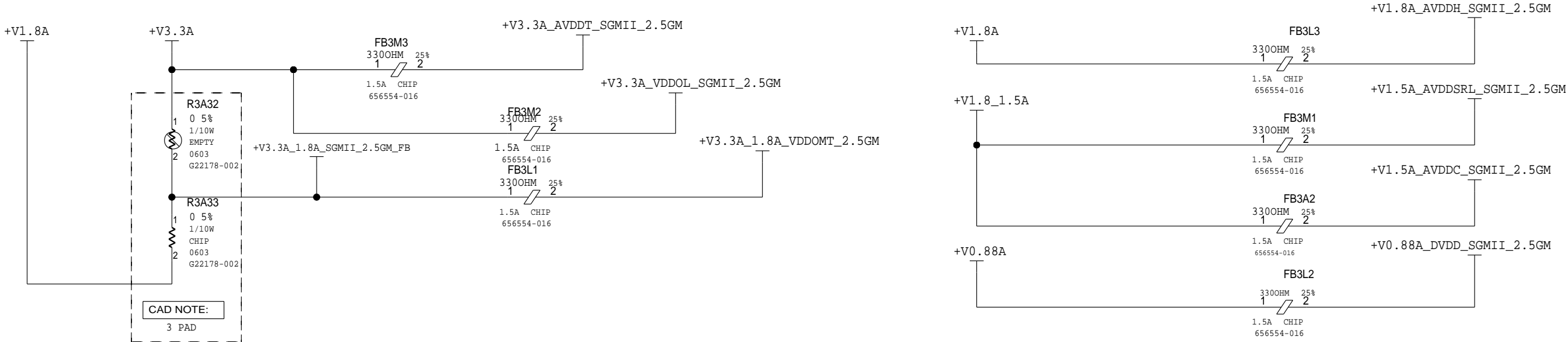




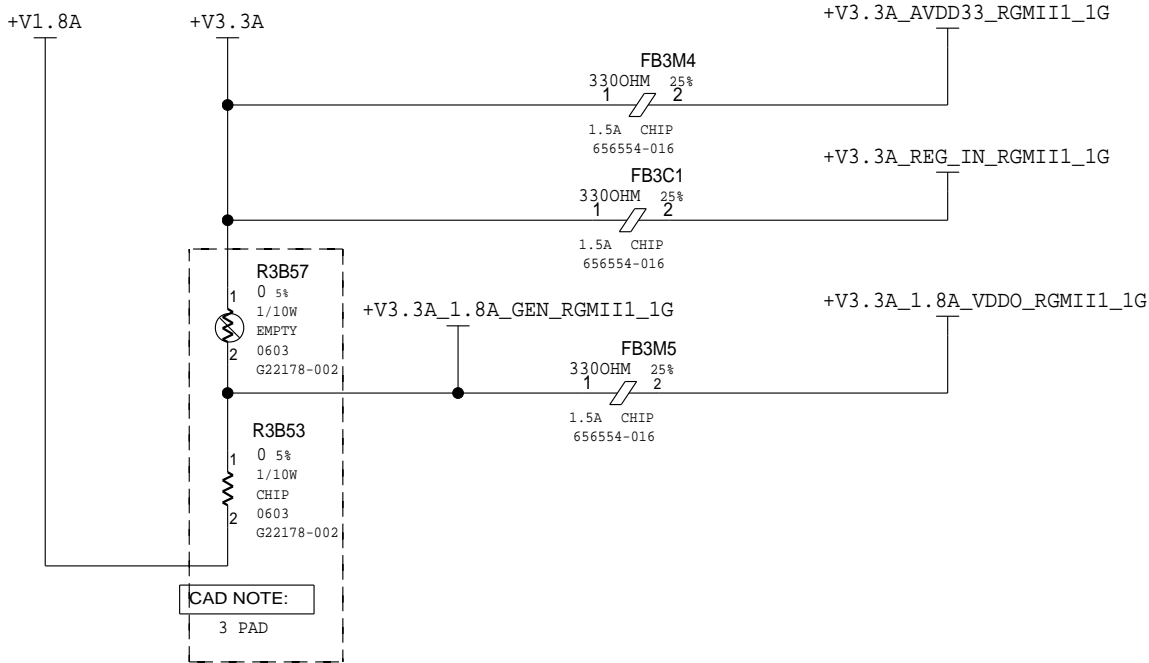
SGMII 2.5G MARVEL PHY RJ45 CONNECTOR INTERFACE (MDI)

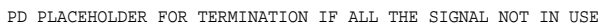


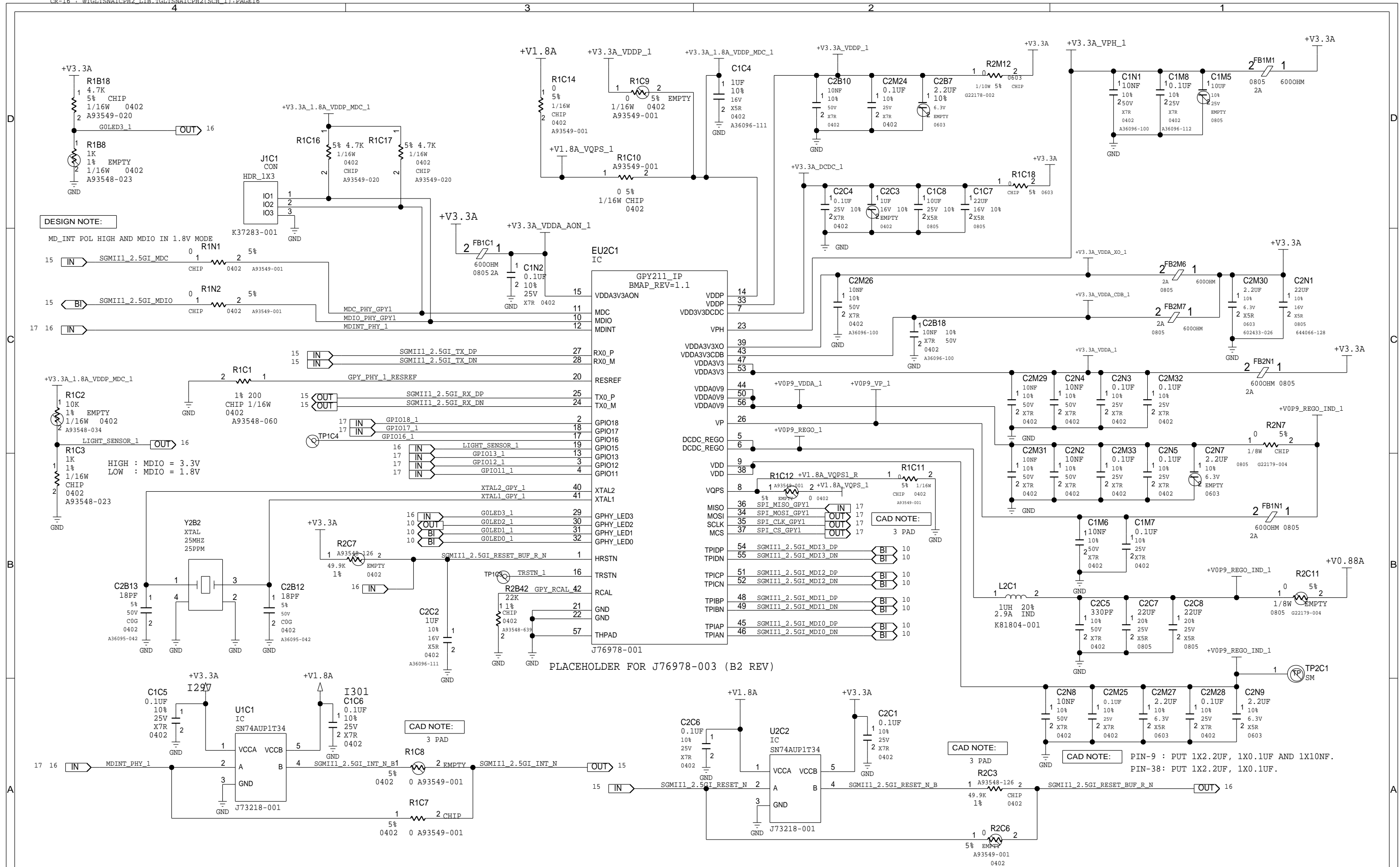
SGMII 2.5G MARVEL PHY POWER FILTERING



RGMI1 1G MARVEL PHY POWER FILTERING







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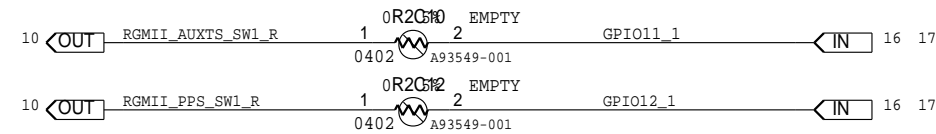
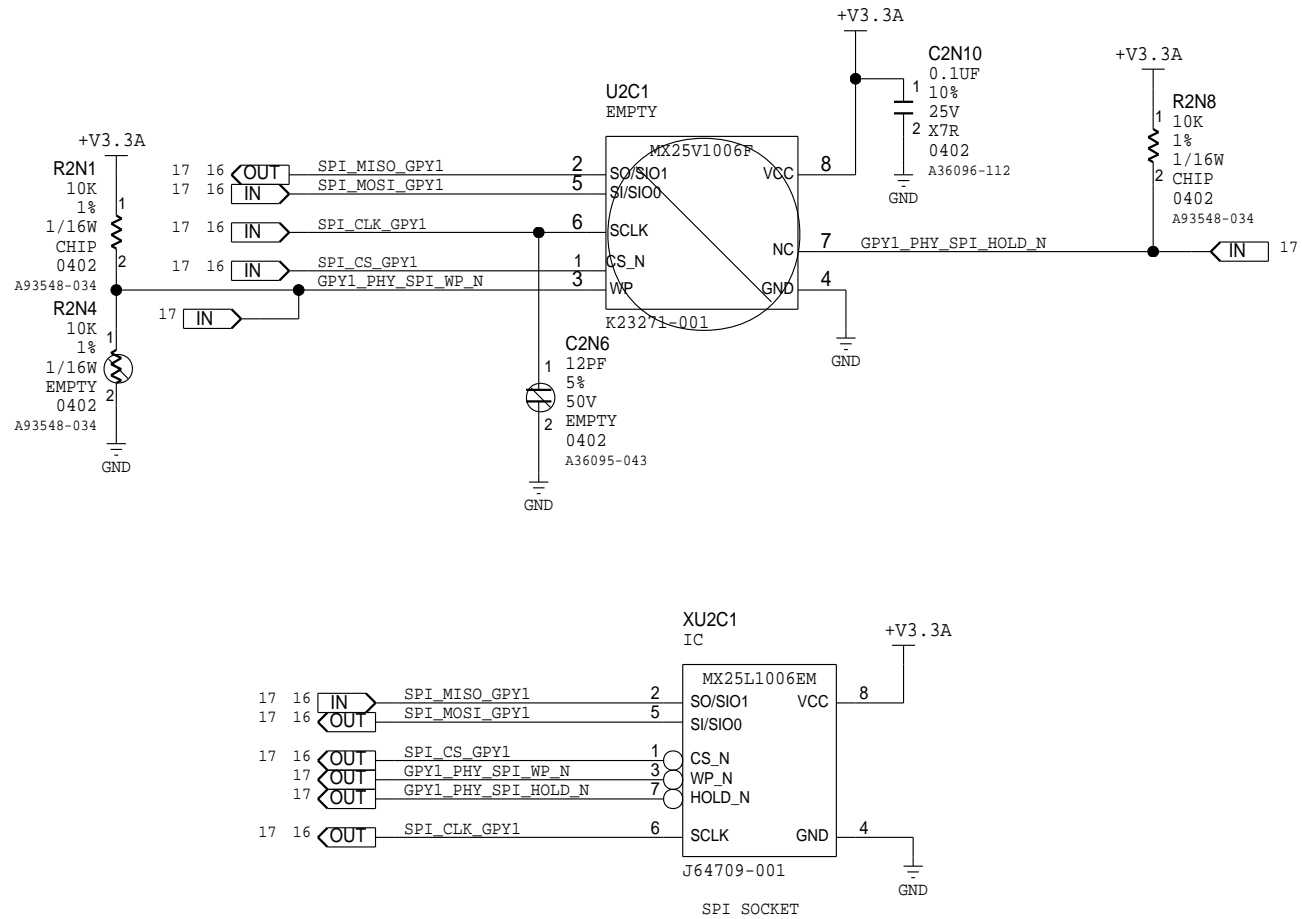
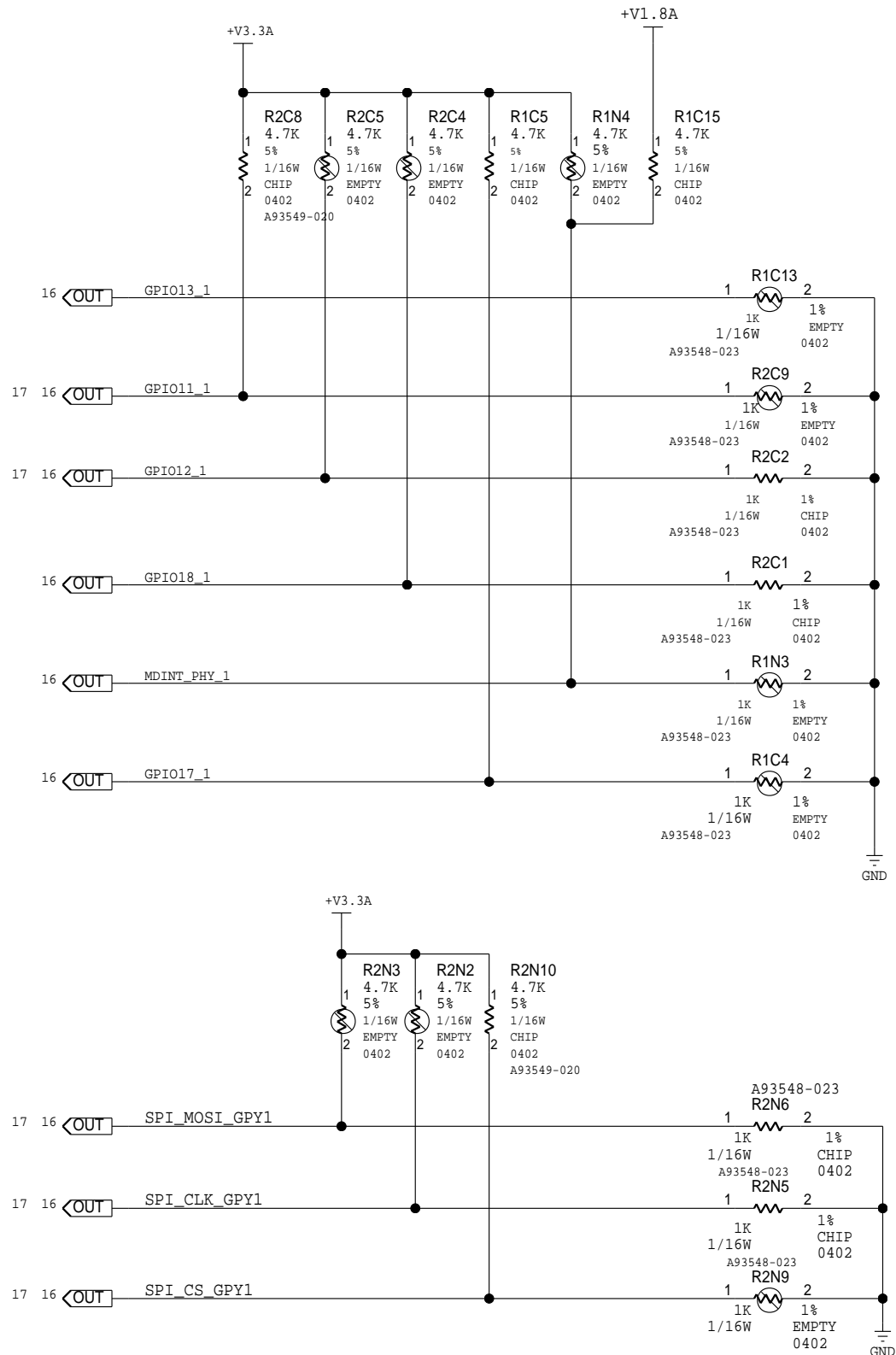
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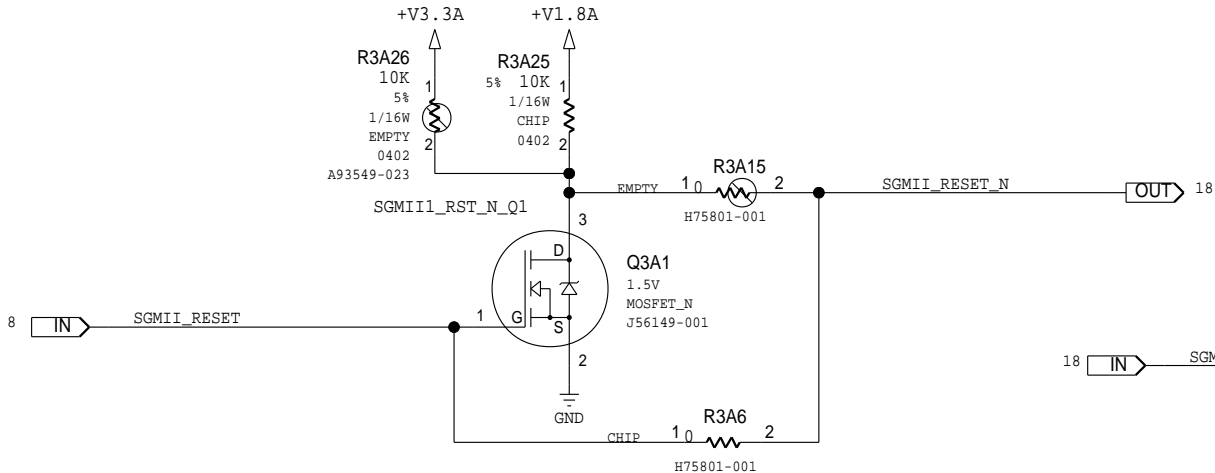
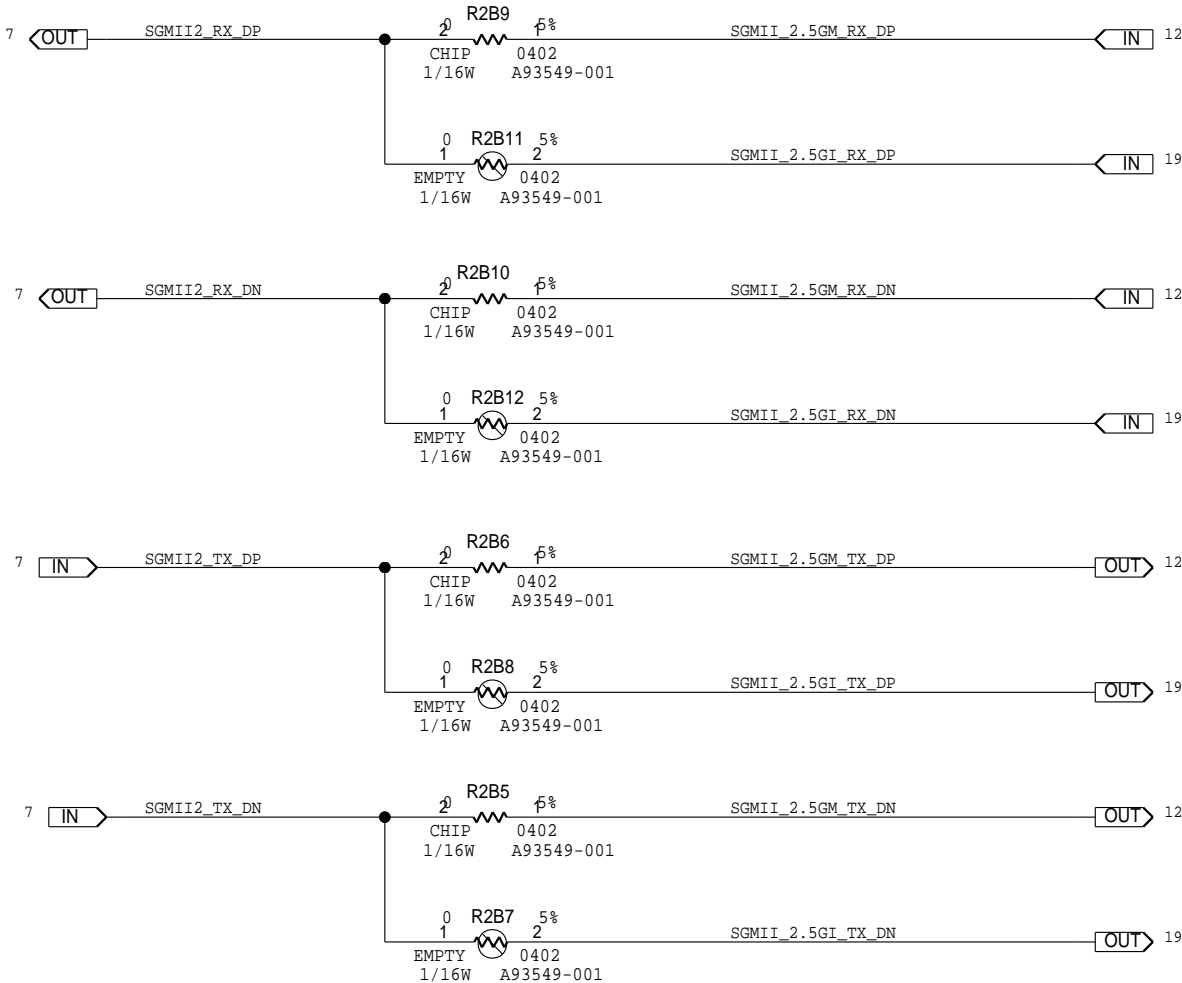
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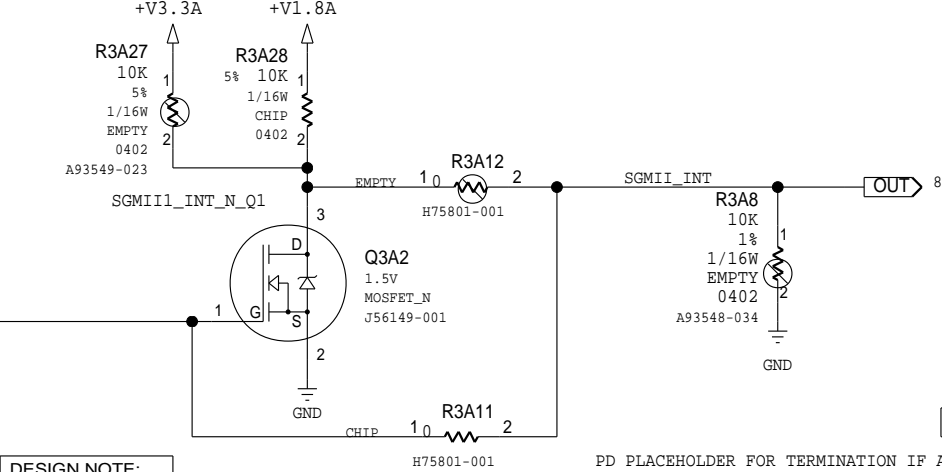
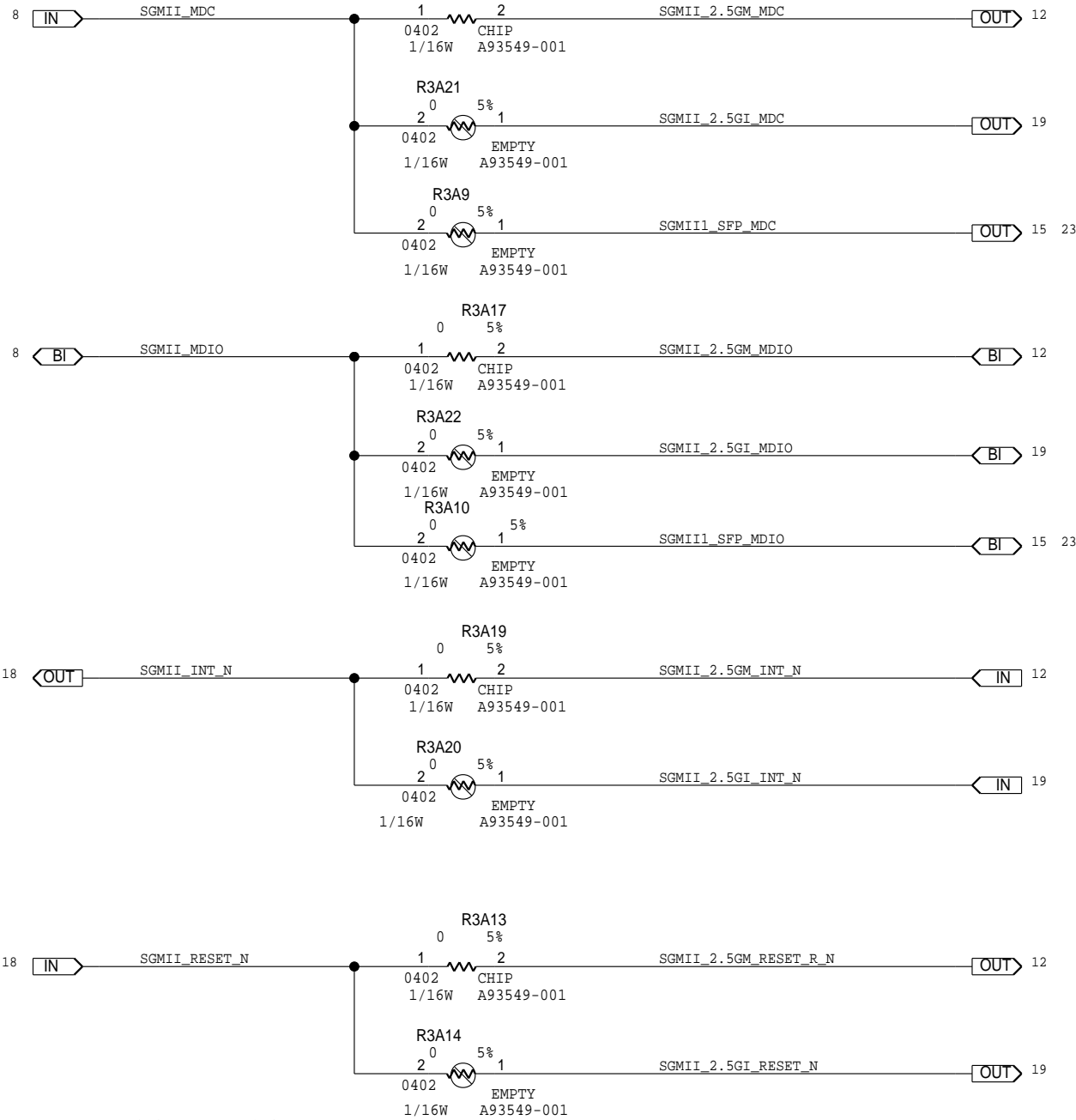
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CAD NOTE:
3 PAD



CAD NOTE:
3 PAD

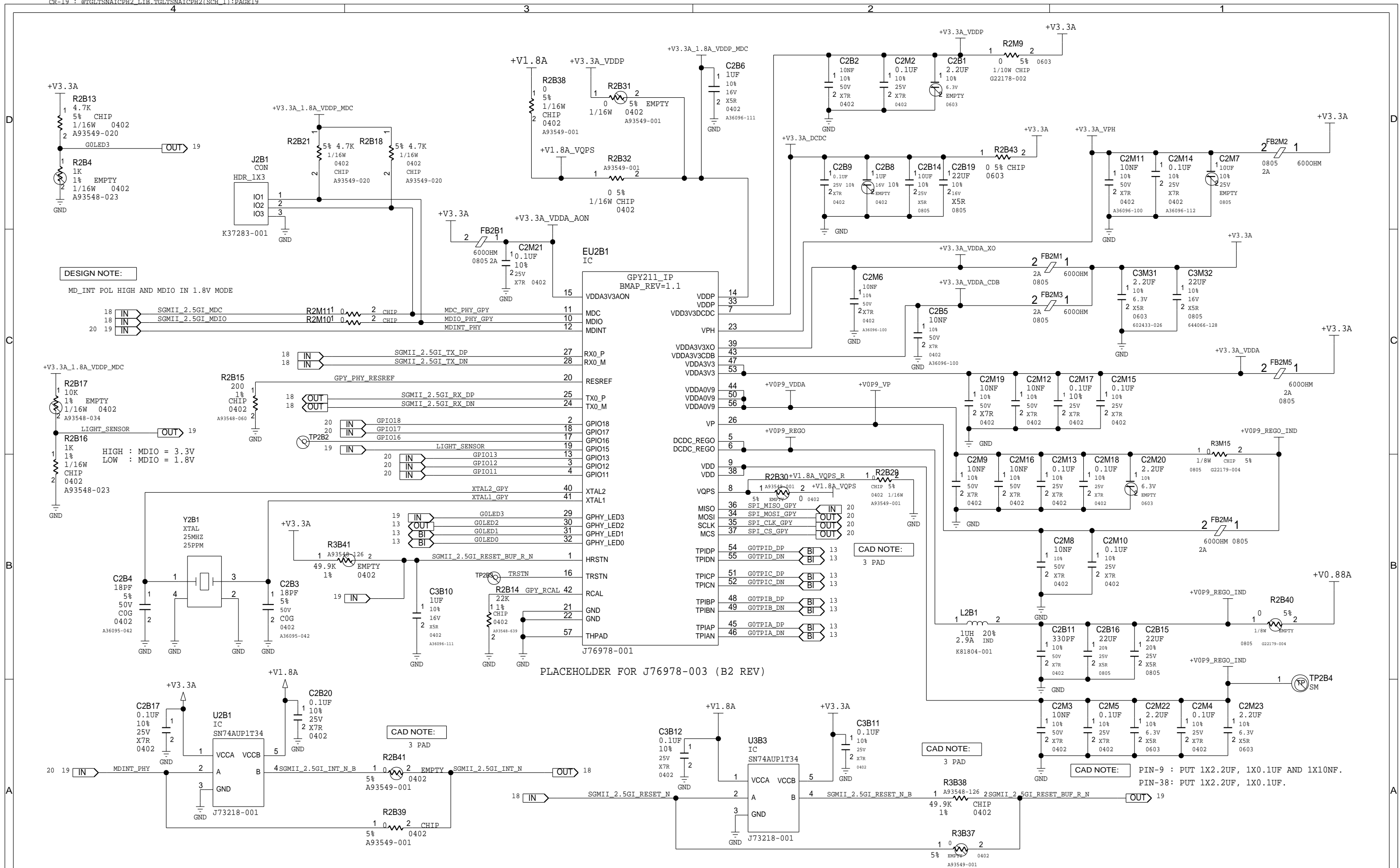


DESIGN NOTE:

DEFENSIVE OPTION FOR GPY211 REV A2

DESIGN NOTE:

PD PLACEHOLDER FOR TERMINATION IF ALL THE SIGNAL NOT IN USE



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