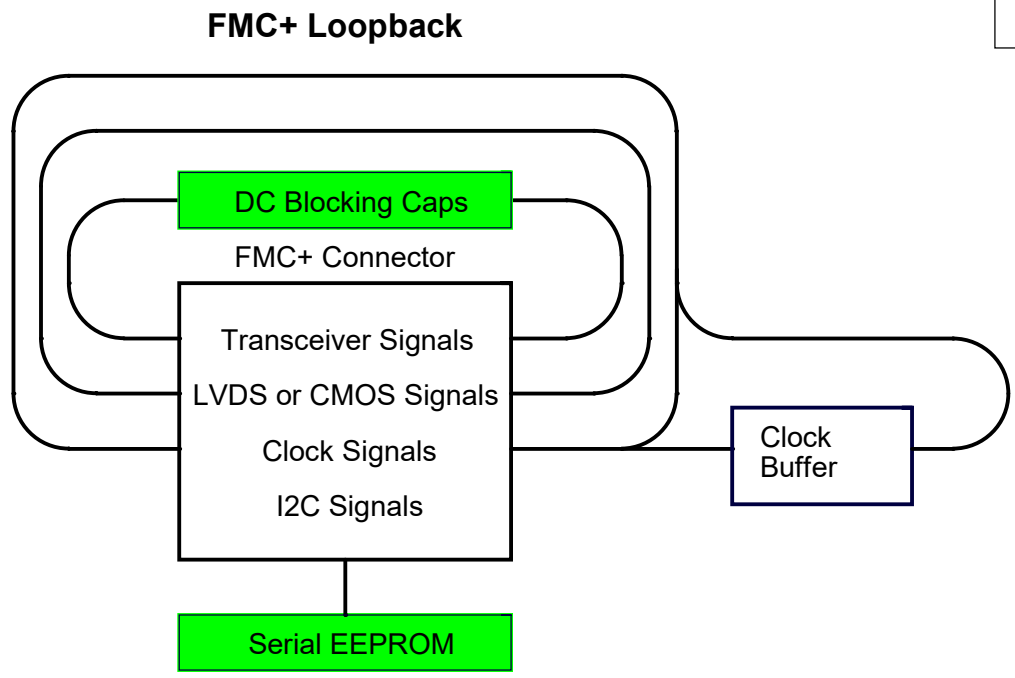


NOTES:

1. Project Drawing Numbers:
- | | |
|--------------------------|----------------|
| Raw PCB | 100-0330631-A1 |
| Gerber Files | 110-0330631-A1 |
| PCB Design Files | 120-0330631-A1 |
| Assembly Drawing | 130-0330631-A1 |
| Fab Drawing | 140-0330631-A1 |
| Schematic Drawing | 150-0330631-A1 |
| PCB Film | 160-0330631-A1 |
| Bill of Materials | 170-0330631-A1 |
| Schematic Design Files | 180-0330631-A1 |
| Functional Specification | 210-0330631-A1 |
| PCB Layout Guidelines | 220-0330631-A1 |
| Assembly Rework | 320-0330631-A1 |
2. The FMC+ pinout was based on v57d4-1d0t-2016-Mar-17, table 5-1.
3. This board was designed for Stratix 10 SI Development kit rev A.

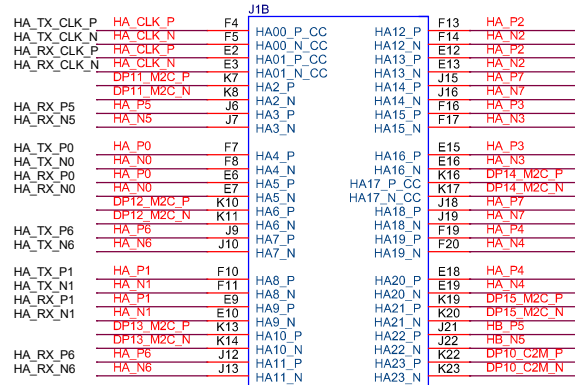
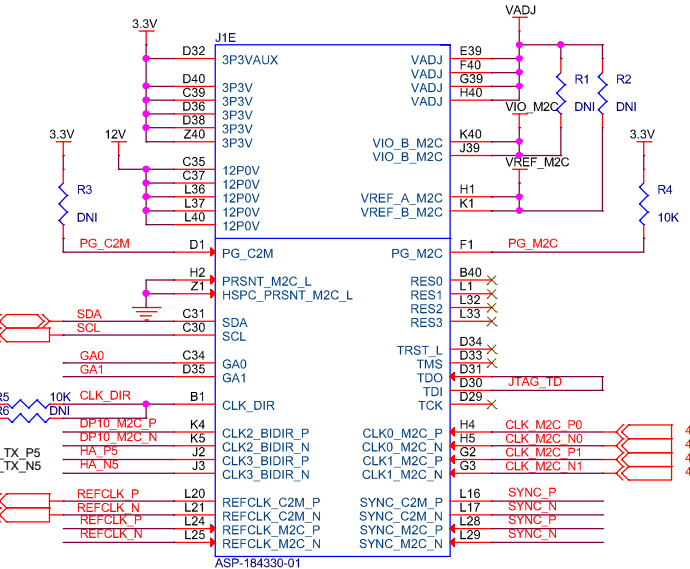
REV	DATE	PAGES	DESCRIPTION
01	07/22/16	All	Preliminary

PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History
2	FMC+ LA / HA / HB
3	FMC+ DP
4	Clock Buffer



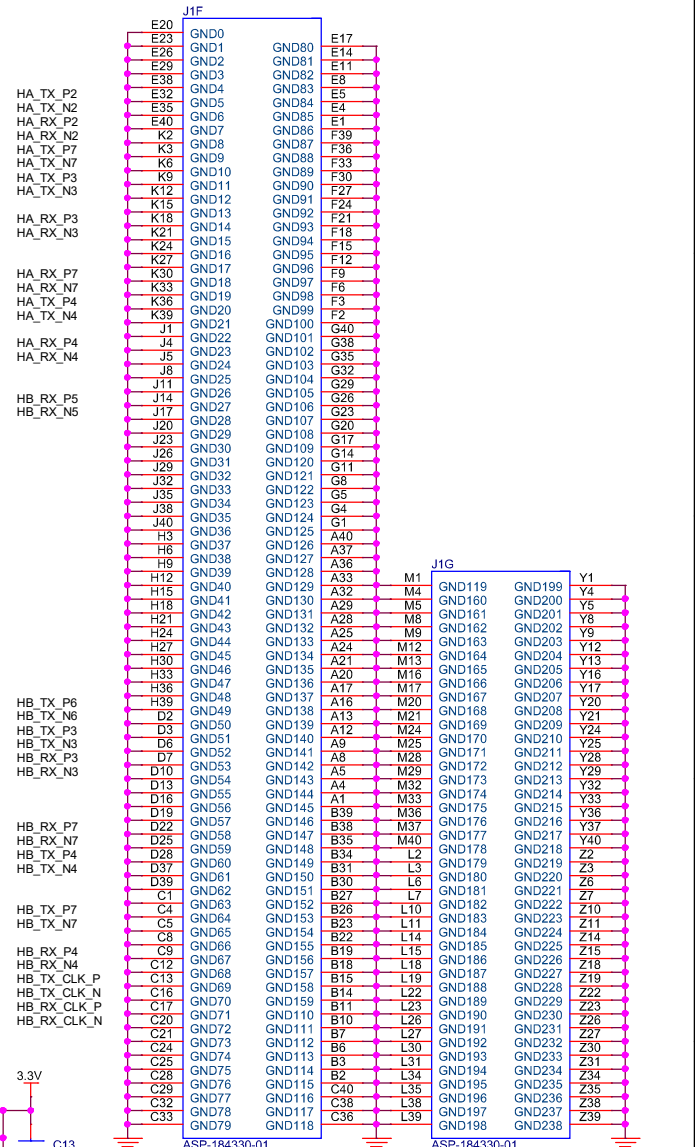
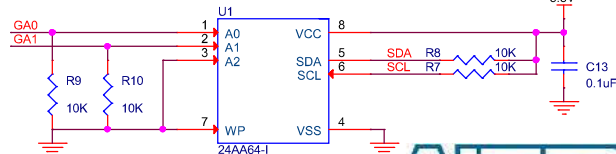
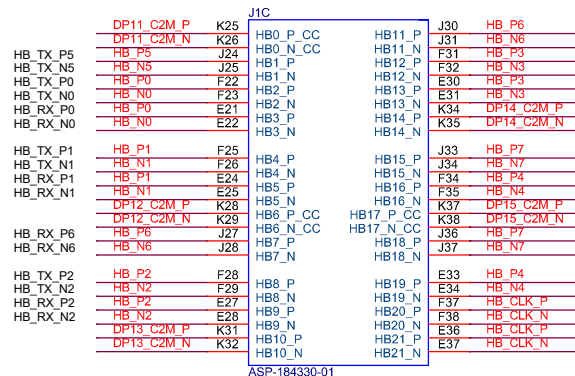
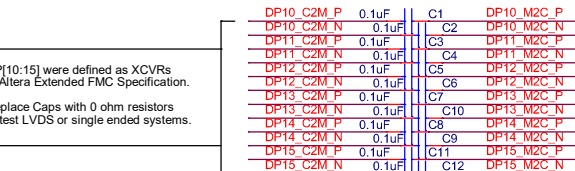
LA[33:0]/HA[23:0]/HB[21:0] loopback are following the Altera Extended FMC Specification, which are backward compatible with FMC loopback card pinout.

J1A				J1B			
	LA CLK_P	G6	LA00_P_CC	LA17_P_CC	D20	LA_P8	LA_TX_P8
	LA CLK_N	G7	LA00_N_CC	LA17_N_CC	D21	LA_N8	LA_TX_N8
	H0ST_CLK_P	D8	LA01_P_CC	LA18_P_CC	C22	LA_P7	LA_RX_P7
	H0ST_CLK_N	D9	LA01_N_CC	LA18_N_CC	C23	LA_N7	LA_RX_N7
TX_P6	LA P6	H7	LA02_P	LA19_P	H22	LA_P9	LA_TX_P9
TX_N0	LA N0	H8	LA02_N	LA19_N	H23	LA_N9	LA_TX_N9
RX_P0	LA P0	G9	LA03_P	LA19_N	G21	LA_P8	LA_RX_P8
RX_N0	LA N0	G10	LA03_N	LA20_P	G22	LA_N8	LA_RX_N8
				LA20_N			
TX_P1	LA P1	H10	LA04_P	LA21_P	H25	LA_P10	LA_TX_P10
TX_N1	LA N1	H11	LA04_N	LA21_P	H26	LA_N10	LA_TX_N10
TX_P2	LA P2	D11	LA05_P	LA22_P	G24	LA_P9	LA_RX_P9
TX_N2	LA N2	D12	LA05_N	LA22_N	G25	LA_N9	LA_RX_N9
RX_P1	LA P1	C10	LA06_P	LA22_N	D23	LA_P11	LA_TX_P11
RX_N1	LA N1	C11	LA06_N	LA23_P	D24	LA_N11	LA_TX_N11
TX_P3	LA P3	H13	LA07_P	LA23_N	H28	LA_P12	LA_TX_P12
TX_N3	LA N3	H14	LA07_N	LA24_P	H29	LA_N12	LA_TX_N12
				LA24_N			
RX_P2	LA P2	G12	LA08_P	LA25_P	G27	LA_P10	LA_RX_P10
RX_N2	LA N2	G13	LA08_N	LA25_N	G28	LA_N10	LA_RX_N10
TX_P4	LA P4	D14	LA09_P	LA26_P	D26	LA_P13	LA_TX_P13
TX_N4	LA N4	D15	LA09_N	LA26_N	D27	LA_N13	LA_TX_N13
RX_P3	LA P3	C14	LA10_P	LA27_P	C26	LA_P11	LA_RX_P11
RX_N3	LA N3	C15	LA10_N	LA27_N	C27	LA_N11	LA_RX_N11
TX_P5	LA P5	H16	LA11_P	LA28_P	H31	LA_P14	LA_TX_P14
TX_N5	LA N5	H17	LA11_N	LA28_N	H32	LA_N14	LA_TX_N14
RX_P4	LA P4	G15	LA12_P	LA29_P	G30	LA_P12	LA_RX_P12
RX_N4	LA N4	G16	LA12_N	LA29_P	G31	LA_N12	LA_RX_N12
TX_P6	LA P6	D17	LA13_P	LA30_P	H34	LA_P15	LA_TX_P15
TX_N6	LA N6	D18	LA13_N	LA30_N	H35	LA_N15	LA_TX_N15
RX_P5	LA P5	C18	LA14_P	LA31_P	G33	LA_P13	LA_RX_P13
RX_N5	LA N5	C19	LA14_N	LA31_N	G34	LA_N13	LA_RX_N13
TX_P7	LA P7	H19	LA15_P	LA32_P	H37	LA_P15	LA_TX_P15
TX_N7	LA N7	H20	LA15_N	LA32_P	H38	LA_N15	LA_TX_N15
RX_P6	LA P6	G18	LA16_P	LA33_P	G36	LA_P14	LA_RX_P14
RX_N6	LA N6	G19	LA16_N	LA33_N	G37	LA_N14	LA_RX_N14



DP[10:15] were defined as XCVRs in Altera Extended FMC Specification.

Replace Caps with 0 ohm resistors to test LVDS or single ended systems.



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FMC+ DP

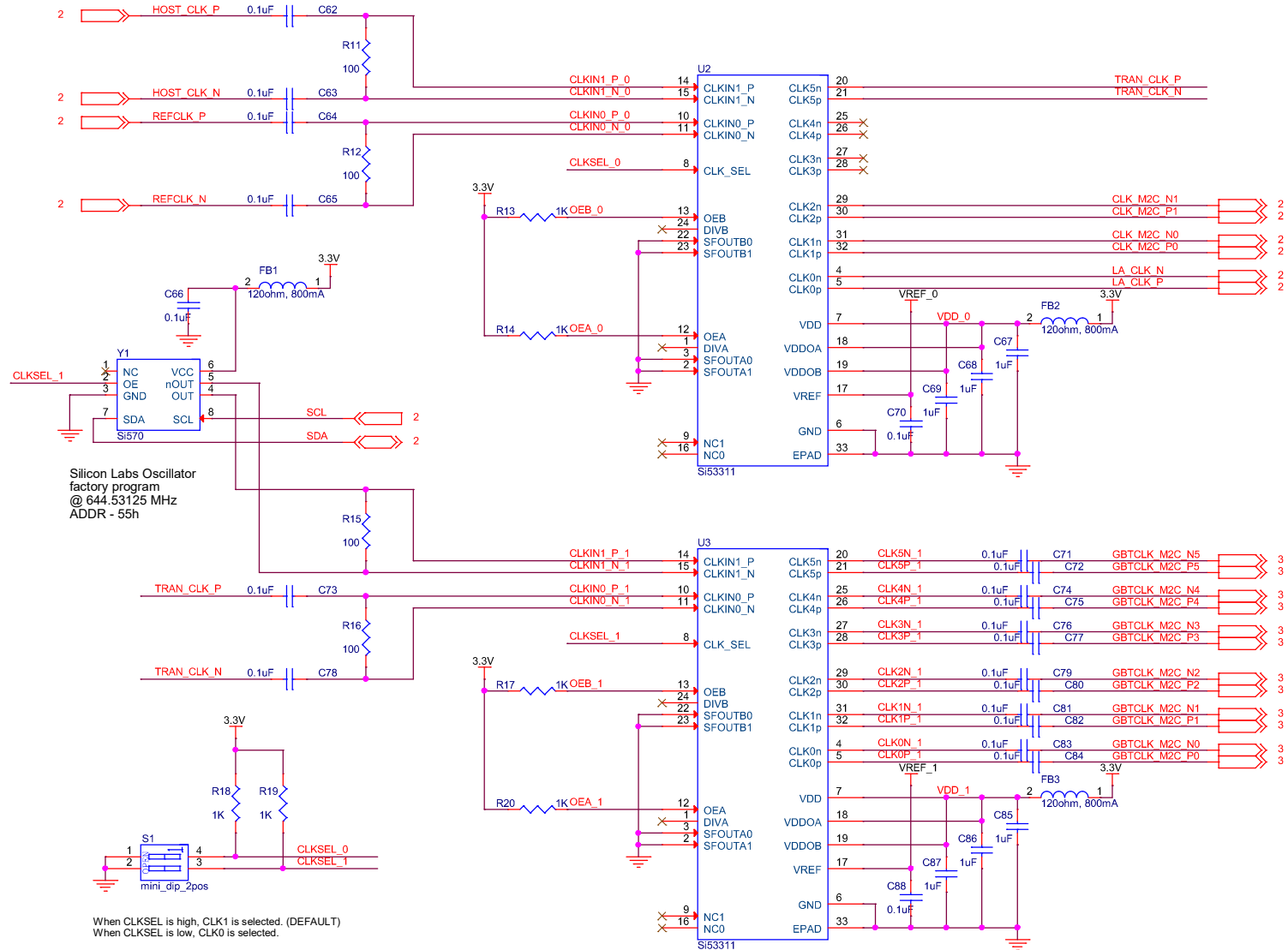
J10			
DP_C2M_P0	C2	DP0_C2M_P	DP0_M2C_P
DP_C2M_N0	C3	DP0_C2M_N	DP0_M2C_N
DP_C2M_P1	A22	DP1_C2M_P	DP1_M2C_P
DP_C2M_N1	A23	DP1_C2M_N	DP1_M2C_N
DP_C2M_P2	A26	DP2_C2M_P	DP2_M2C_P
DP_C2M_N2	A27	DP2_C2M_N	DP2_M2C_N
DP_C2M_P3	A30	DP3_C2M_P	DP3_M2C_P
DP_C2M_N3	A31	DP3_C2M_N	DP3_M2C_N
DP_C2M_P4	A34	DP4_C2M_P	DP4_M2C_P
DP_C2M_N4	A35	DP4_C2M_N	DP4_M2C_N
DP_C2M_P5	A38	DP5_C2M_P	DP5_M2C_P
DP_C2M_N5	A39	DP5_C2M_N	DP5_M2C_N
DP_C2M_P6	B36	DP6_C2M_P	DP6_M2C_P
DP_C2M_N6	B37	DP6_C2M_N	DP6_M2C_N
DP_C2M_P7	B32	DP7_C2M_P	DP7_M2C_P
DP_C2M_N7	B33	DP7_C2M_N	DP7_M2C_N
DP_C2M_P8	B28	DP8_C2M_P	DP8_M2C_P
DP_C2M_N8	B29	DP8_C2M_N	DP8_M2C_N
DP_C2M_P9	B24	DP9_C2M_P	DP9_M2C_P
DP_C2M_N9	B25	DP9_C2M_N	DP9_M2C_N
DP_C2M_P10	Z24	DP10_C2M_P	DP10_M2C_P
DP_C2M_N10	Z25	DP10_C2M_N	DP10_M2C_N
DP_C2M_P11	Y26	DP11_C2M_P	DP11_M2C_P
DP_C2M_N11	Y27	DP11_C2M_N	DP11_M2C_N
DP_C2M_P12	Z28	DP12_C2M_P	DP12_M2C_P
DP_C2M_N12	Z29	DP12_C2M_N	DP12_M2C_N
DP_C2M_P13	Y30	DP13_C2M_P	DP13_M2C_P
DP_C2M_N13	Y31	DP13_C2M_N	DP13_M2C_N
DP_C2M_P14	M18	DP14_C2M_P	DP14_M2C_P
DP_C2M_N14	M19	DP14_C2M_N	DP14_M2C_N
DP_C2M_P15	M22	DP15_C2M_P	DP15_M2C_P
DP_C2M_N15	M23	DP15_C2M_N	DP15_M2C_N
DP_C2M_P16	M26	DP16_C2M_P	DP16_M2C_P
DP_C2M_N16	M27	DP16_C2M_N	DP16_M2C_N
DP_C2M_P17	M30	DP17_C2M_P	DP17_M2C_P
DP_C2M_N17	M31	DP17_C2M_N	DP17_M2C_N
DP_C2M_P18	M34	DP18_C2M_P	DP18_M2C_P
DP_C2M_N18	M35	DP18_C2M_N	DP18_M2C_N
DP_C2M_P19	M38	DP19_C2M_P	DP19_M2C_P
DP_C2M_N19	M39	DP19_C2M_N	DP19_M2C_N
DP_C2M_P20	Z8	DP20_C2M_P	DP20_M2C_P
DP_C2M_N20	Z9	DP20_C2M_N	DP20_M2C_N
DP_C2M_P21	Y6	DP21_C2M_P	DP21_M2C_P
DP_C2M_N21	Y7	DP21_C2M_N	DP21_M2C_N
DP_C2M_P22	Z4	DP22_C2M_P	DP22_M2C_P
DP_C2M_N22	Z5	DP22_C2M_N	DP22_M2C_N
DP_C2M_P23	Y2	DP23_C2M_P	DP23_M2C_P
DP_C2M_N23	Y3	DP23_C2M_N	DP23_M2C_N
4	GBTCLK_M2C_P3	GBTCLK3_M2C_P	GBTCLK0_M2C_P
4	GBTCLK_M2C_N3	GBTCLK3_M2C_N	GBTCLK0_M2C_N
4	GBTCLK_M2C_P4	GBTCLK4_M2C_P	GBTCLK1_M2C_P
4	GBTCLK_M2C_N4	GBTCLK4_M2C_N	GBTCLK1_M2C_N
4	GBTCLK_M2C_P5	GBTCLK5_M2C_P	GBTCLK2_M2C_P
4	GBTCLK_M2C_N5	GBTCLK5_M2C_N	GBTCLK2_M2C_N

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Clock Buffer



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